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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/684,449	10/15/2003	Shoji Kawahito	0020-5186P	8839

2292 7590 10/18/2004

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EXAMINER	
NGUYEN, MINH T	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 10/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/684,449	KAWAHITO ET AL.	
	Examiner	Art Unit	
	Minh Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-7* is/are allowed.

6)☒ Claim(s) *8 and 9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/15/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Objections

2. Claims 3-5 and 8-9 are objected to because of the following informalities:

In claim 3, line 7, "multiphase clock signal" should be changed to -- multiphase clock signals --, see lines 1-2 of claim 1.

In claim 4, line 7, "multiphase clock signal" should be changed to -- multiphase clock signals --, see lines 1-2 of claim 1.

In claim 5, line 5, "first pulse signal" should be changed to -- second pulse signal --, see Fig. 5, block D1, signal Ssp);

line 7, "second pulse signal" should be changed to -- first pulse signal --, see Fig. 5, block D1, signal Smp).

In claim 8, line 14, "internal clock signal" should be changed to -- internal clock signals --, see line 10.

In claim 9, line 4, "multiphase clock signal" should be changed to -- multiphase clock signals --, see lines 1-2 of claim 8.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 8-9 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent No. 5,087,829, issued to Ishibashi et al.

As per claim 8, Ishibashi discloses a clock signal generation circuit (Fig. 1b) for generating multiphase clock signals (Fig. 10, CK0, ..., CK3) in accordance with a master clock signal (the reference clock from the input buffer 40, column 6, lines 54-55) having a predetermined frequency, comprising:

a common clock generation circuit section (Fig. 1b, block 41 which comprises variable delay circuit 51) adapted to generate a third delay signal (Fig. 11a, the delay signal at one of the outputs of delays 1107-1109) obtained by delaying the master clock signal (the reference clock) by a third delay time (the delay time of delays 1121, 1107-1109, column 12, lines 63-65) and generate a third pulse signal (Fig. 11a, the signal at the output of OR gate 1115, column 13, lines 6-7) having a pulse width of the third delay time in accordance with the master clock signal and the third delay signal;

a multiphase clock generation circuit section (Fig. 1b, block 56, Fig. 10 is the detail) adapted to generate multiphase internal clock signals (Fig. 10, the clock signals which are fed to

the inputs of AND gates 1010-1013) in accordance with the master clock signal (it is clear that these signals are generated based on the reference signal); and

a clock control circuit section (Fig. 1b, blocks 55, 57 and 58) constituted by clock control circuits (AND gates 1010-1013) each for controlling a change point of a signal level of corresponding one of the internal clock signal outputted from the multiphase clock generation circuit section to be coincident with a change point of a signal level of the third pulse signal (Fig. 1b, the delay time detection circuit 58, the delay control circuit 57 and phase comparator 1008 in Fig. 10 performs the recited function).

As per claim 9, Ishibashi further discloses each of the clock control circuits comprises:

an output circuit (Fig. 10, for example AND gate 1013) for outputting a clock signal (CK0) which forms the multiphase clock signals (CK0, ..., CK3) in accordance with a corresponding internal clock signal (the internal clock signal which is fed to one of the input terminals of the AND gate 1013) outputted from the multiphase clock signal generation circuit; and

an output control circuit (the delay control circuit 57 for controlling the variable delay element 1000) for controlling an output signal level of one of the clock signals outputted from the output circuit in accordance with the third pulse signal.

Allowable Subject Matter

4. Claims 1-7 are allowed after amended to correct the informality objections noted above.

Claims 1-7 are allowed because the prior art of record fails to disclose or suggest the inclusion of slave DLL circuits wherein each slave DLL circuit is configured to perform the function recited on the last six lines of claim 1.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Minh Nguyen whose telephone number is **571-272-1748**. The examiner can normally be reached on Monday, Tuesday, Thursday, Friday 7:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

10/12/04

Minh Nguyen
Primary Examiner
Art Unit 2816